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INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

EXAMINER	
CLARK, SHEILA V	
ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/640,961	MA ET AL.	
	Examiner	Art Unit	
	S. V. Clark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,24-29,31 and 33-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,24-29, 31 and 33-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9-28-2009, 7-7-2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung.

Chung teaches in for example figures 6-8 a microelectronic package, comprising: a microelectronic die 140 having an active surface and at least one side; encapsulation material 150 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface (see figure 7 where at least the left the side surface of encapsulant 150 is shown having a planar side surface running parallel to the planar side surface of die 140 and therefore obviously "planar to"); a first dielectric material layer 146 disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and at least one first conductive trace 144 disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

With regard to claim 2, the microelectronic package of claim 1, further including at least one second dielectric material layer 120 disposed over said at least one first

conductive trace and said first dielectric material layer.

With regard to claim 3, the microelectronic package of claim 2, wherein at least a portion of at least one second conductive trace 132b extends through and resides on said at least one second dielectric material layer.

With regard to claim 4, the microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

Thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art. To therefore incorporate a at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Chung would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 25, he microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die (see figure 7 where at least the left the bottom surface of encapsulant 150 is shown having a planar side surface running parallel to the planar back side surface of die 140 and therefore

obviously"planar to").

Claims 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung.

Chung shows a microelectronic package, comprising:
a microelectronic die having an active surface 140, a back surface, and at least one side; and encapsulation material 150 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface (see figure 7 where at least the bottom side surfaces of encapsulant 150 are shown having a planar side surface running parallel to the back surface of die 140 and therefore obviously "planar to").

Thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art. To therefore incorporate a at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Chung would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 27, the microelectronic package of claim 26, further including at least one first conductive trace 140 (or 110 or 132a) disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic

die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

With regard to claim 28, the microelectronic package of claim 27, further including at least one second dielectric material layer (120) disposed over said at least one first conductive trace and said first dielectric material layer.

With regard to claim 29, the microelectronic package of claim 28, wherein at least a portion of at least one second conductive trace (132a) extends through and resides on said at least one second dielectric material layer.

Claims 31, 33, 34, 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung.

Chung teaches in for example figures 6-8 and 14 microelectronic package, comprising: a plurality of microelectronic dice (see figure 14) each having an active surface and at least one side, encapsulation material 150 adjacent said at least one microelectronic die side of said plurality of microelectronic dice, wherein said encapsulation material includes at least one surface substantially planar to said plurality of microelectronic dice active surfaces (see figure 7 where at least the left the side surface of encapsulant 150 is shown having a planar side surface running parallel to the planar side surface of die 140 and therefore obviously "planar to"); , and at least one

first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace 144 extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

With regard to claim 33, the microelectronic package of claim 31 further including at least one second dielectric material layer 120 disposed over said at least one first conductive trace and said first dielectric material layer.

With regard to claim 34, the microelectronic package of claim 33, wherein at least a portion of at least one second conductive trace 132a extends through and resides on said at least one second dielectric material layer.

With regard to claim 35, (Previously Presented) The microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

Thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art. To therefore incorporate a at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Chung would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 37, the microelectronic package of claim 31, wherein the microelectronic die further includes a back surface, and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die active surface (see figure 7 where at least the top side surface of encapsulant 150 is shown having a planar side surface running parallel to the planar active side surface of die 140 and therefore obviously"planar to").

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Fordemwalt et al.

Fordemwalt et al shows in for example figure 1 in microelectronic package, comprising: a microelectronic die 13 having an active surface and at least one side; encapsulation material 12 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one top surface shown substantially planar to said microelectronic die active surface; a first dielectric material layer 21 disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and at least one first conductive trace (25 or (22, 23, 24, 25) disposed on said first dielectric material layer and in physical and electrical contact with

said microelectronic die active surface(see col. 4, lines 56-59), wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Claims 26, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fordemwalt et al.

Fordemwalt et al shows in for example figure 1 a microelectronic package, comprising: a microelectronic die 13 having an active surface, a back surface, and at least one side; and encapsulation material 12 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one top surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface (see figure 1 where at least the bottom side surface of encapsulant 12 is shown having a planar side surface running parallel to the planar back side surface of die 13 and therefore obviously "planar to").

Though Fordemwalt et al fails to show a heat dissipation device in thermal contact with the back surface of the chip thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art and a typical standard in this art. To therefore incorporate a at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Fordemwalt et al would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claims 27, the microelectronic package of claim 26, further including at least one first conductive trace (25 or (22, 23, 24, 25) disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface (see col. 4, lines 56-59), wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Claim 31 is rejected under 35 U.S.C. 102(b) as being anticipated by Fordemwalt et al.

Fordemwalt et al shows in for example figure 1 a microelectronic package, comprising: a plurality of microelectronic dice (13, 14, 15, 16) each having an active surface and at least one side, encapsulation material 12 adjacent said at least one microelectronic die side of said plurality of microelectronic dice, wherein said encapsulation material includes at least one top surface substantially planar to said plurality of microelectronic dice active surfaces, and at least one first conductive trace (25 or (22, 23, 24, 25) disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface(see col. 4, lines 56-59) , wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

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Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Nishihara et al.

Nishihara shows in for example figure 3 (figure 7) a microelectronic package, comprising: a microelectronic die 1 having an active surface and at least one side; encapsulation material 8 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one bottom surface substantially planar to said microelectronic die active surface; a first dielectric material layer 3 disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and at least one first conductive trace 2 disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Claims 26, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishihara et al.

. Nishihara shows in for example figure 3 a microelectronic package, comprising: a microelectronic die 1 having an active surface, a back surface, and at least one side; and encapsulation material 8 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one bottom surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface.

Though Nishihara et al fails to show a heat dissipation device in thermal contact

with the back surface of the chip thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art and a typical standard in this art to improve thermal dissipation. To therefore incorporate a at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Nishihara et al would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 27, the microelectronic package of claim 26, further including at least one first conductive trace 4 disposed on said first dielectric material layer 3 and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Claims 1, 4, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Donovan.

Donovan shows a microelectronic package, comprising:
a microelectronic die 12b having an active surface and at least one side;
encapsulation material 28 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one top surface substantially planar to said microelectronic die active surface; 23 a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material

surface; and at least one first conductive trace 32 disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

With regard to claims 4, the microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device 40 thermal contact with said microelectronic device.

With regard to claim 24, the microelectronic package of claim 4, wherein said encapsulation material is shown adjacent at least a portion of said at least one heat dissipation device.

Claims 26, 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Donovan.

Donovan shows a microelectronic package, comprising:
a microelectronic die 12b having an active surface, a back surface, and at least one side; and encapsulation material 28 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one top surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface and at least one heat dissipation device 40 is shown in thermal contact with said microelectronic die back surface.

With regard to claim 27, the microelectronic package of claim 26, further including at least one first conductive trace 32 disposed on said first dielectric material

layer 23 and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Claims 31, 35, 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Donovan

Donovan shows a microelectronic package, comprising:

a plurality of microelectronic dice (12a, 12b, 12c) each having an active surface and at least one side, encapsulation material 28 adjacent said at least one microelectronic die side of said plurality of microelectronic dice, wherein said encapsulation material includes at least one top surface substantially planar to said plurality of microelectronic dice active surfaces, and at least one first conductive trace 32 disposed on said first dielectric material layer 23 and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

With regard to claim 35, the microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation 40 device in thermal contact with said microelectronic die back surface.

With regard to claim 36, the microelectronic package of claim 35, wherein said encapsulation material is shown adjacent at least a portion of said at least one heat dissipation device.

Claim 38 is rejected under 35 U.S.C. 102(b) as being anticipated by Donovan

Donovan shows a microelectronic package, comprising:

a microelectronic die 12b having an active surface, a back surface, and at least one side; encapsulation material 28 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one top surface substantially planar to said microelectronic die active surface; a first dielectric material layer 23 disposed on at least a portion of said microelectronic die active surface and said encapsulation, material surface; at least one first conductive trace 32 disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface; and at least one heat dissipation device 40 in thermal contact with said microelectronic die back surface.

Claims 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung.

Chung teaches in for example figures 6-8 a microelectronic package, comprising: a microelectronic die 140 having an active surface and at least one side;

encapsulation material 150 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface (see figure 7 where at least the left the side surface of encapsulant 150 is shown having a planar side surface running parallel to the planar side surface of die 140 and therefore obviously "planar to"); a first dielectric material layer 146 disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and at least one first conductive trace 144 disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art. To therefore incorporate a at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Chung would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 39, the microelectronic package of claim 38, further including: at least one second dielectric material layer 120 disposed over said at least one first conductive trace and said first dielectric material layer, wherein at least a portion of at least one second conductive trace 132b extends through and resides on

said at least one second dielectric material layer.

With regard to claim 40, the microelectronic package of claim 39, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device (see obvious above).

Claims 4, 24, 35, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung or Nishihara or Fordemwalt et al (as applied above) in view of Donovan et al.

The features of the claims from which claims 4, 24, 35, and 36 depend have been discussed in detail supra except for use of a heat dissipation device in thermal contact with the bottom surface of the microelectronic chip. Donovan teaches a similar device to those of Chung or Nishihara or Fordemwalt et al and teaches the use of heat dissipation device 40 formed in thermal contact with the back of microelectronic device 12c (12 a and 12b). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a heat dissipation device on the bottom surface of the electronic device. The ordinary artisan would have been motivated to modify Chung or Nishihara or Fordemwalt for the purposes of improving or increasing heat dissipation. Further providing the bottom surfaces of electronic devices with heat dissipation structures to improve heat dissipation is well known and performed conventionally in this art.

Claims 1-4, 24-29, 31, 33-40 are rejected.

Applicant's arguments filed 11-9-2009 have been fully considered but they are not persuasive. The prior art relied upon in the rejection are deemed to continue to teach the features of the invention as they are broadly recited primarily item for item. Heat sinks are commonly attached to back surfaces of chips and this type of features would have been considered very well known to one having ordinary skill in this art and Donovan teaches this features formed on the back of the chip. Chung's trace was identified as item 144 which is clearly shown to be in physical and electrical contact with the active surface and though item 144 was identified as a bump, bumps are metal layers may be characterized in many forms and fashioned into trace like shapes (metal layers). Further the term trace also fails to limit the feature to one type of form or shape. Trace can be a metal layer which also can be representative of a bump. The term "planar to" also fails to define one fixed structural arrangement. "Planar to" is not considered the same as "planar with" nor "coplanar with", etc. If the applicant persists with the planar details it is suggested that they must be more descriptive in their structural details.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. V. Clark whose telephone number is (571) 272-1725. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. V. Clark/
Primary Examiner, Art Unit 2823
January 30, 2010